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(71)Applicant : **KOYANAGI MITSUMASA**
FUJI XEROX CO LTD
(72)Inventor : **KOYANAGI MITSUMASA**
OKANO TAISUKE
MIYAGAWA NOBUAKI

(54) METHOD OF MANUFACTURING THREE-DIMENSIONAL IMAGE PROCESSOR

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a manufacturing method for a three-dimensional image processor which can sharply simplify the manufacture process due to needlessness of mounting and removal process of a supporting board, can manufacture a three-dimensional image processor by simple and easy process, and can form embedded wiring surrounded by a highly reliable insulating film.
SOLUTION: A transparent substrate 10 made of quartz glass, where many microlenses 12 are made two-dimensionally, is bonded to a photoelectric transfer substrate 20 where a

photodiode and a MOS transistor are made on an n-type silicon crystalline substrate 16 wherein an insulating layer 36 consisting of silicon diode is inserted, through an adhesive 14 consisting of high polymer material such as epoxy resin, polyimide resin, or the like, so that the main face of the photoelectric transfer substrate 20 and the rear of the transparent substrate 10 may oppose to each other.

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CLAIMS

[Claim(s)]

[Claim 1] The manufacture approach of a three-dimension image processing system of pasting up the transparence substrate equipped with the lens which condenses light, and the photo-electric-translation substrate which was electrically connected to this optoelectric transducer while the optoelectric transducer was formed in the principal plane and with which it embedded and wiring was formed so that the rear face of a transparence substrate and the principal plane of a photo-electric-translation substrate may counter, and manufacturing a three-dimension image processing system.

[Claim 2] The manufacture approach of a three-dimension image processing system according to claim 1 of grinding the rear-face side of said photo-electric-translation substrate, exposing said embedding wiring, pasting up so that the magnification conversion substrate which was electrically connected to this amplifier and the analog-to-digital converter and with which it embedded and wiring was formed may be electrically connected to the outcrop of said embedding wiring in this amplifier and an analog-to-digital converter while an amplifier and an analog-to-digital converter are formed in the rear face of this photo-electric-translation substrate at a principal plane, and manufacturing a three-dimension image processing system.

[Claim 3] The manufacture approach of a three-dimension image processing system according to claim 2 of grinding the rear-face side of said magnification conversion substrate, exposing said embedding wiring, pasting up so that the data storage substrate which was electrically connected to this data storage while data storage was formed in the rear face of this magnification conversion substrate at the principal plane and with which it embedded and wiring was formed may be electrically connected to the outcrop of said embedding wiring in this data storage, and manufacturing a three-dimension image processing system.
[Claim 4] The manufacture approach of a three-dimension image processing system according to claim 3 of grinding the rear-face side of said data storage substrate, exposing said embedding wiring, pasting up so that the data-processing substrate which was electrically connected to this data processor while the data processor was formed in the rear face of this data storage substrate at the principal plane and with which it embedded and wiring was formed may be electrically connected to the outcrop of said embedding wiring in this data processor, and manufacturing a three-dimension image processing system.
[Claim 5] The manufacture approach of a three-dimension image processing system according to claim 4 of grinding the rear-face side of said data-processing substrate, exposing said embedding wiring, pasting up so that the output circuit substrate which was electrically connected to this output circuit while the output circuit was formed in the rear face of this data-processing substrate at the principal plane and with which it embedded and wiring was formed may be electrically connected to the outcrop of said embedding wiring in this output circuit, and manufacturing a three-dimension image processing system.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the manufacture approach of a three-dimension image processing system.
[0002]
[Description of the Prior Art] In recent years, development of the three-dimension semiconductor integrated circuit equipment which accumulated two or more circuitry blocks in three dimensions is furthered from the objects, such as high integration, densification, etc. of semiconductor integrated circuit equipment. Especially the three-dimension image processing system (intelligent image processor) that unified the digital disposal circuit for processing image sensors and its signal carries out high-speed processing of the image data obtained from a photosensor at juxtaposition, and since it becomes possible to obtain a high-definition image on real time, it has many hope.
[0003] Although the manufacture had been considered by the monolithic method which repeats SOI substrate formation and formation of the semiconductor device to a SOI substrate using the SOI (Silicon On Insulator) technique by laser recrystallization etc. at the beginning, these three-dimensions semiconductor integrated circuit equipment had

problems, like production time with difficult crystalline reservation is long, in order to have carried out the laminating of the SOI to the multilayer.
[0004] For this reason, the manufacture approach of the three-dimension semiconductor integrated circuit equipment by the lamination technique which sticks the single crystal semiconductor substrates by which a semiconductor device or semiconductor integrated circuit equipment was produced beforehand is considered variously.
[0005] The CUBIC technique which sticks the semi-conductor substrate thin-film-ized by polish as a kind of a lamination technique on a monthly semiconductor world (1990 year 9 month number p58-64, such as wood Yoshihiro) is proposed. With a CUBIC technique, after pasting up the 1st semi-conductor substrate with which the semiconductor device was first formed on the silicon substrate on a support substrate, polishing of the excessive silicon substrate is carried out, and it is thin-film-ized. Next, wiring required for connection of the lengthwise direction of devices, such as embedding wiring, backwiring, and a contact member that consists of a bump/a pool, is formed, and the 1st semi-conductor substrate and the 2nd semi-conductor substrate with which the semiconductor device was formed on the silicon substrate are stuck. And finally a support substrate is removed and the semiconductor device of multilayer structure is completed.
[0006] Moreover, the manufacture approach of the three-dimension semiconductor integrated circuit equipment by the lamination technique is indicated by JP,6-260594,A. Although the point which carries out polishing of the excessive silicon substrate, and thin-film-izes it is common on the CUBIC technique after this approach pastes up the 1st semi-conductor substrate with which the semiconductor device was formed on the silicon substrate on a support substrate The point that the deep groove for forming embedding wiring in the 1st semi-conductor substrate beforehand is prepared, And it differs from the CUBIC technique at the point which removes a support substrate for the 1st semi-conductor substrate and the 2nd semi-conductor substrate with which the semiconductor device was formed on the silicon substrate after lamination and lamination, and forms embedding wiring.
[0007]
[Problem(s) to be Solved by the Invention] However, any manufacture approach includes the process which exfoliates lamination in a support substrate, and exfoliates the 1st semi-conductor substrate from a support substrate in the 1st semi-conductor substrate after grinding, and had the problem that a production process was complicated. Since it is necessary to form the transparence substrate equipped with the micro lens which constitutes image sensors in the front face after removing a support substrate to manufacture a three-dimension image processing system especially, a production process becomes complicated still more.
[0008] Moreover, with a CUBIC technique, in order to remove a support substrate after carrying out polishing of the excessive silicon substrate and thin-film-izing it, when removing a support substrate, there was a problem that the integrated circuit formed on the semi-conductor substrate was damaged.
[0009] moreover, by the approach indicated by JP,6-260594,A In order to paste up the 1st semi-conductor substrate with which the deep groove for forming embedding wiring was prepared beforehand on a support substrate, In order to oxidize the side attachment wall of a deep groove and to form an insulator layer, after pasting up the problem that clearance of the adhesives which entered the deep groove is difficult, and the 1st semi-

conductor substrate and the 2nd semi-conductor substrate, Oxidation temperature could not be raised beyond the heat-resistant temperature of adhesives, but there was a problem that a reliable insulator layer could not be formed.

[0010] This invention is made in view of the trouble of the above-mentioned conventional technique, the object of this invention has the unnecessary attachment-and-detachment process of a support substrate, a production process can be simplified substantially, and it is in offering the manufacture approach of a three-dimension image processing system that a three-dimension image processing system can be manufactured according to a simple and easy process. Moreover, other objects of this invention are to offer the manufacture approach of the three-dimension image processing system which was surrounded by the reliable insulator layer and which can embed and can form wiring.

[0011]

[Means for Solving the Problem] In order to attain the above-mentioned object, the manufacture approach of a three-dimension image processing system according to claim 1 is characterized by pasting up the transparence substrate equipped with the lens which condenses light, and the photo-electric-translation substrate which was electrically connected to this optoelectric transducer while the optoelectric transducer was formed in the principal plane and with which it embedded and wiring was formed so that the rear face of a transparence substrate and the principal plane of a photo-electric-translation substrate may counter, and manufacturing a three-dimension image processing system.

[0012] The transparence substrate equipped with the lens which condenses light in invention of claim 1, without using a support substrate etc., In order to paste up the photo-electric-translation substrate which was electrically connected to this optoelectric transducer and with which it embedded and wiring was formed so that the rear face of a transparence substrate and the principal plane of a photo-electric-translation substrate may counter while an optoelectric transducer is formed in a principal plane, A transparence substrate can be used as a transparence substrate of image sensors as it is, and the adhesion process to a support substrate, the clearance process from a support substrate, and the formation process of a transparence substrate are unnecessary, and can simplify substantially the production process of a three-dimension image processing system. Moreover, since it sticks with a transparence substrate after embedding at a photo-electric-translation substrate and forming wiring, embedding wiring surrounded by the reliable insulator layer can be formed.

[0013] The manufacture approach of a three-dimension image processing system according to claim 2 In invention of claim 1, grind the rear-face side of said photo-electric-translation substrate, and said embedding wiring is exposed. The magnification conversion substrate which was electrically connected to this amplifier and the analog-to-digital converter while the amplifier and the analog-to-digital converter were formed in the principal plane at the rear face of this photo-electric-translation substrate and with which it embedded and wiring was formed It is characterized by pasting up so that this amplifier and an analog-to-digital converter may be electrically connected to the outcrop of said embedding wiring, and manufacturing a three-dimension image processing system.

[0014] According to invention of claim 2, the three-dimension image processing system which carried out the laminating of the magnification conversion substrate which was electrically connected to the amplifier and the analog-to-digital converter according to the simple and easy process of polish and adhesion, and with which it embedded and wiring

was formed to the image-sensors section which consists of a transparence substrate and a photo-electric-translation substrate can be manufactured.
[0015] The manufacture approach of a three-dimension image processing system according to claim 3 In invention of claim 2, grind the rear-face side of said magnification conversion substrate, and said embedding wiring is exposed. The data storage substrate which was electrically connected to this data storage while data storage was formed in the principal plane at the rear face of this magnification conversion substrate and with which it embedded and wiring was formed It is characterized by pasting up so that this data storage may be electrically connected to the outcrop of said embedding wiring, and manufacturing a three-dimension image processing system.
[0016] According to invention of claim 3, the three-dimension image processing system which carried out the laminating of the data storage substrate which was electrically connected to data storage while the store was formed in the principal plane of the simple and easy process of polish and adhesion, and with which it embedded and wiring was formed to the layered product by which the magnification conversion substrate was formed in the image-sensors section which consists of a transparence substrate and a photo-electric-translation substrate of polish and adhesion can be manufactured.
[0017] The manufacture approach of a three-dimension image processing system according to claim 4 In invention of claim 2, grind the rear-face side of said data storage substrate, and said embedding wiring is exposed. The data-processing substrate which was electrically connected to this data processor while the data processor was formed in the principal plane at the rear face of this data storage substrate and with which it embedded and wiring was formed It is characterized by pasting up so that this data processor may be electrically connected to the outcrop of said embedding wiring, and manufacturing a three-dimension image processing system.
[0018] According to invention of claim 4, the three-dimension image processing system which carried out the laminating of the data-processing substrate which was electrically connected to this data processor while the data processor was formed in the principal plane of the simple and easy process of polish and adhesion, and with which it embedded and wiring was formed to the layered product by which the magnification conversion substrate and the data storage substrate were formed in the image-sensors section which consists of a transparence substrate and a photo-electric-translation substrate of polish and adhesion can be manufactured.
[0019] The manufacture approach of a three-dimension image processing system according to claim 5 In invention of claim 4, grind the rear-face side of said data-processing substrate, and said embedding wiring is exposed. This output circuit pastes up the output circuit substrate which was electrically connected to this output circuit while the output circuit was formed in the principal plane and with which it embedded and wiring was formed on the rear face of this data-processing substrate so that it may connect with the outcrop of said embedding wiring electrically. It is characterized by manufacturing a three-dimension image processing system.
[0020] According to invention of claim 5, the three-dimension image processing system which carried out the laminating of the output circuit substrate which was electrically connected to the layered product by which the magnification conversion substrate, the data-storage substrate, and the data processor were formed in the image-sensors section which consists of a transparence substrate and a photo-electric-translation substrate of

polish and adhesion according to it in this output circuit while the output circuit was formed in the principal plane of the simple and easy process of polish and adhesion, and with which it embedded and wiring was formed can be manufactured.
[0021]
[Embodiment of the Invention] Hereafter, the manufacture approach of the three-dimension image processing system of this invention is explained concretely, referring to a drawing. Drawing 1 - drawing 5 are the sectional views showing each process of the manufacture approach of the three-dimension image processing system of this invention.
[0022] First, as shown in drawing 1 , the transparence substrate 10 made from quartz glass with which many micro lenses 12 were formed in the shape of two-dimensional is pasted up on the photo-electric-translation substrate 20 through the adhesives 14 which consist of polymeric materials, such as an epoxy resin and polyimide resin, so that the principal plane of the photo-electric-translation substrate 20 and the rear face of the transparence substrate 10 may counter.
[0023] The photo-electric-translation substrate 20 used above forms a photodiode and an MOS transistor on n mold silicon crystal substrate 16 with which the insulating layer 36 which consists of NI silicon oxide was inserted in the interior. A photodiode forms p mold impurity layer 18 on n mold silicon crystal substrate 16 of the photo-electric-translation substrate 20, and is formed by forming n mold impurity layer 22 in the field corresponding to the focal location of the micro lens 12 of p mold impurity layer 18 surface. Moreover, the MOS transistor is formed by forming n mold impurity layer 22 used as the source and a drain in parts other than the image pick-up field of p mold impurity layer 18 surface, and forming the gate electrode 26 which consists of polish recon mutually insulated by insulator layer 24A on p mold impurity layer 18 between this n mold impurity layer 22. In addition, the adjoining MOS transistor is separated by the component demarcation membrane 30 which consists of NI silicon oxide.
[0024] Moreover, the trench (deep groove) which penetrates the component demarcation membrane 30 and arrives at the rear face of the photo-electric-translation substrate 20 is prepared in the photo-electric-translation substrate 20. In addition, such a trench can be formed by inductive-coupling mold plasma etching etc. An insulator layer 32 is formed in the internal surface of this trench, in the trench, it fills up with an electrical conducting material, and embeds, and wiring 34 is formed. As an electrical conducting material which forms the embedding wiring 34, metals of low resistance, such as low resistance polycrystalline silicon which doped the impurity, for example, and a tungsten, are used.
[0025] It connects with the source electrode 28 which consists of aluminum, and gets down, and n mold impurity layer 22 used as the source of an MOS transistor is connected to the drain electrode 29 with which n mold impurity layer 22 used as a drain was insulated with the source electrode 28 by insulator layer 24B and which consists of aluminum, for example. This drain electrode 29 is embedded, and is connected to wiring 34, and the charge accumulated in the photodiode which consists of an n-type channel 22 and a p mold impurity layer 18 is transmitted to the amplifier later mentioned through this embedding wiring 34 by impressing a predetermined electrical potential difference to the gate electrode 26.
[0026] Next, as shown in drawing 2 , the photo-electric-translation substrate 20 adhered to the transparence substrate 10 is ground from a rear-face side by chemical mechanical polishing, and is thin-film-ized. In the NI silicon oxide which constitutes the insulating

layer 36 inserted in n mold silicon crystal substrate 16, since polish resistance is larger than silicon, polish stops before an insulating layer 36, and the embedding wiring 34 is exposed from an insulating layer 36. Although the transparence substrate 10 plays the role of a support substrate at this time, since the transparence substrate made from quartz glass which unified and formed the micro lens 12 from the beginning is used, it is not necessary to remove later.

[0027] The image-sensors section equipped with the transparence substrate 10 equipped with the lens which condenses light according to the above process, and the photo-electric-translation substrate 20 is completed.

[0028] Next, as shown in drawing 3 , the magnification conversion substrate 40 which changes into a digital signal the analog signal amplified while amplifying the signal from the photo-electric-translation substrate 20 is pasted up on the rear face of the photo-electric-translation substrate 20. This magnification conversion substrate 40 forms gate 44A insulated by insulator layer 42A, source 46A, and two or more MOSFET50A (two MOSFETs are illustrated with the gestalt of this operation) which consists of drain 48A on silicon substrate 38A by which insulating-layer 36A which consists of NI silicon oxide was inserted in the interior. MOSFET50A which these-adjoins is separated by component demarcation membrane 52A which consists of NI silicon oxide.

[0029] Moreover, the trench which penetrates this component demarcation membrane 52A, and reaches a circuit side from the rear-face side front face of the magnification conversion substrate 40 is prepared in the magnification conversion substrate 40. Insulator layer 54A is formed in the internal surface of this trench, in the trench, it fills up with an electrical conducting material, and embeds, and wiring 56A is formed. As an electrical conducting material which forms embedding wiring 56A, metals of low resistance, such as low resistance polycrystalline silicon which doped the impurity, for example, and a tungsten, are used. Direct continuation of the aluminum wiring 58A is carried out to the edge by the side of the circuit side of this embedding wiring 56A. The integrated circuit which contains an amplifier (amplifier) and an analog-to-digital converter (ADC) by this is constituted. The formed integrated circuit is covered with insulator layer 60A which consists of NI silicon oxide, and flattening of the front face by the side of the integrated circuit of the magnification conversion substrate 40 is carried out. Moreover, aluminum wiring 58A is pulled out from opening prepared in this insulator layer 60A, and it is exposed to the front face of insulator layer 60A.

[0030] The micro bump 62 is formed in the front face by the side of the rear face of the above-mentioned photo-electric-translation substrate 20 so that the edge of the embedding wiring 34 exposed from the front face of an insulating layer 36 may be contacted. On the other hand, the micro bump 64 is formed also in the front face of insulator layer 60A or front face by the side of the integrated circuit of the magnification conversion substrate 40 so that the edge of exposed aluminum wiring 58A may be contacted. A micro bump can form by the lift off which used the resist mask, and can use the alloy or indium of gold and an indium as a micro bump's ingredient.

[0031] Temporary adhesion of the photo-electric-translation substrate 20 is piled up and carried out on the magnification conversion substrate 40 so that the micro bump 62 prepared in the front face by the side of the rear face of the photo-electric-translation substrate 20 and the micro bump 64 prepared in the front face by the side of the integrated-circuit side of the magnification conversion substrate 40 may be connected

electrically. In addition, the alignment equipment using the infrared radiation which penetrates a silicon wafer can perform alignment of the photo-electric-translation substrate 20 and the magnification conversion substrate 40.
[0032] The photo-electric-translation substrate 20 which carried out temporary adhesion, and the magnification conversion substrate 40 are put into the chamber in which pressurization is possible with the container holding a liquefied epoxy resin, the photo-electric-translation substrate 20 and the magnification conversion substrate 40 which made the inside of a chamber the vacuum and carried out temporary adhesion are dipped into a liquefied epoxy resin, it returns to ordinary pressure, and an epoxy resin 66 is poured into the clearance between substrates. A substrate is pulled up after that, an epoxy resin 66 is stiffened, and adhesion with the magnification conversion substrate 40 and the photo-electric-translation substrate 20 is completed.
[0033] Next, as shown in drawing 4 , from a rear-face side, the magnification conversion substrate 40 is ground in uniform thickness by chemical mechanical polishing, and is thin-film-ized. Since polish resistance is larger than silicon, as for the NI silicon oxide which constitutes insulating-layer 36A, embedding wiring 56A in which polish stops before insulating-layer 36A, and is formed to the location deeper than insulating-layer 36A is exposed from insulating-layer 36A.
[0034] Next, as shown in drawing 5 , the data storage substrate 70 equipped with the data storage (register array) which memorizes data temporarily is pasted up on the rear face of the magnification conversion substrate 40 adhered to the photo-electric-translation substrate 20. The data storage substrate 70 used here on silicon substrate 38B by which insulating-layer 36B which consists of NI silicon oxide was inserted in the interior like the magnification conversion substrate 40 Gate 44B insulated by insulator layer 42B, source 46B, and two or more MOSFET50B (two MOSFETs are illustrated with the gestalt of this operation) which consists of drain 48B are formed. Adjoining MOSFET50B is separated by component demarcation membrane 52B which consists of NI silicon oxide.
[0035] Moreover, the trench which penetrates this component demarcation membrane 52B, and reaches a circuit side from the rear-face side front face of the data storage substrate 70 is prepared in the data storage substrate 70. Insulator layer 54B is formed in the internal surface of this trench, in the trench, it fills up with an electrical conducting material, and embeds, and wiring 56B is formed. As an electrical conducting material which forms embedding wiring 56B, metals of low resistance, such as low resistance polycrystalline silicon which doped the impurity, for example, and a tungsten, are used. Direct continuation of the aluminum wiring 58B is carried out to the edge by the side of the circuit side of embedding wiring 56B. The integrated circuit which contains data storage by this is constituted. The formed integrated circuit is covered with insulator layer 60B which consists of NI silicon oxide, and flattening of the front face by the side of the integrated circuit of the data storage substrate 70 is carried out. Aluminum wiring 58B is pulled out from opening prepared in this insulator layer 60B, and it is exposed to the front face of insulator layer 60B.
[0036] The micro bump 71 is formed in the front face by the side of the rear face of the above-mentioned magnification conversion substrate 40 so that the edge of embedding wiring 56A exposed from the front face of insulating-layer 36A may be contacted. On the other hand, the micro bump 72 is formed also in the front face of insulator layer 60B or

front face by the side of the integrated circuit of the data storage substrate 70 so that the edge of exposed aluminum wiring 58B may be contacted. With and the micro bump 71 prepared in the front face by the side of the rear face of the magnification conversion substrate 40 Temporary adhesion of the magnification conversion substrate 40 is piled up and carried out on the data storage substrate 70 so that the micro bump 72 prepared in the front face by the side of the integrated circuit of the data storage substrate 70 may be connected electrically. The magnification conversion substrate 40 and the data storage substrate 70 are pasted up with an epoxy resin 74 like the case where the photo-electric-translation substrate 20 and the magnification conversion substrate 40 are pasted up.

[0037] Next, as shown in drawing 6 , the data-processing substrate 80, the output circuit substrate 90, and the output terminal section 100 are formed in the rear face of the data storage substrate 70 in order. The data storage substrate 70 adhered to the magnification conversion substrate 40 is ground from a rear-face side like the formation process of the above-mentioned magnification conversion substrate 40 or the data storage substrate 70, and the data-processing substrate 80 with which the embedding wiring 82 was formed in preparation for the rear face of the data storage substrate 70 in the data processor (processor array) is pasted up so that the integrated circuit in which it was prepared by both substrates may embed and wiring 82 may connect electrically. Furthermore, after grinding this data-processing substrate 80 from a rear-face side, the output circuit substrate 90 with which it embedded at the rear face of the data-processing substrate 80, and wiring 92 was formed is pasted up so that the integrated circuit in which it was prepared by both substrates may embed and wiring 92 may connect electrically. And the micro bump 93 is formed so that the edge of the embedding wiring 92 which ground the output circuit substrate 90 from the rear-face side, embedded from the insulator layer of output circuit substrate 90 rear face, was made to expose the edge of wiring 92, and was exposed may be contacted.

[0038] And finally the output terminal section 100 is formed in the rear face of the output circuit substrate 90. The embedding wiring 104 which the output terminal section 100 penetrated this silicon substrate 102 to the silicon substrate 102, and was exposed to substrate both-sides side is formed. As an electrical conducting material which forms the embedding wiring 104, metals of low resistance, such as copper, a tungsten, and gold, are used, for example. The micro bump 94 is formed in the front face of the input side of this output terminal section 100 so that one edge of the embedding wiring 104 exposed from the front face of the insulating layer of the output terminal section 100 may be contacted. And the micro bump 93 prepared in the front face by the side of the rear face of the output circuit substrate 90 and the micro bump 94 prepared in the front face of the input side of the output terminal section 100 contact, and both substrates are pasted up so that the integrated circuit prepared in the output circuit substrate 90 may be electrically connected to the output terminal of the output terminal section 100. And the micro bump 106 is formed in the front face of the output side of the above-mentioned output terminal section 100 so that the other-end section of the embedding wiring 104 may be contacted. The micro bump 106 can form from gold, or indiums or those alloys. Moreover, it is good also as a solder bump.

[0039] The three-dimension image processing system shown in drawing 6 which unified the image-sensors section which consists of the transparence substrate 10 and the photo-electric-translation substrate 20 which were equipped with the lens which condenses light

according to the above process, and the processing section (the magnification conversion substrate 40, the data storage substrate 70, the data-processing substrate 80, and output circuit substrate 90) for processing the signal from the image-sensors section can be obtained.

[0040] With the gestalt of this operation, since many micro lenses paste up a photo-electric-translation substrate on the transparence substrate made from quartz glass formed in the shape of two-dimensional directly, it is not necessary to prepare a support substrate separately, and the attachment-and-detachment process of a support substrate becomes unnecessary. A production process can be simplified substantially by this and a three-dimension image processing system can be manufactured according to a simple and easy process. Moreover, since embedding wiring of each integrated-circuit substrate is formed before lamination, embedding wiring surrounded by the reliable insulator layer can be formed.

[0041] Although the insulating layer which becomes each semi-conductor substrate for forming an integrated circuit from NI silicon oxide used the silicon substrate formed in the interior with the gestalt of the above-mentioned implementation, the silicon substrate which does not contain the insulating layer which consists of NI silicon oxide may be used.

[0042] Although the gestalt of the above-mentioned implementation explained the example which connects electrically the substrate which a micro bump is formed in the both ends of embedding wiring, and micro bumps are contacted, and adjoins, you may make it connect electrically the substrate which forms a micro bump only in one edge of embedding wiring, and adjoins it.

[0043] In the image-sensors section which consists of a transparence substrate and a photo-electric-translation substrate equipped with the condenser lens with the gestalt of the above-mentioned implementation Although the example which forms each processing section of the magnification conversion substrate for processing the signal from the image-sensors section, a data storage substrate, a data-processing substrate, and an output circuit substrate by repeating polish and lamination was explained After grinding and embedding the photo-electric-translation substrate which constitutes the image-sensors section from a rear-face side and exposing wiring, a photo-electric-translation substrate is also connectable with a magnification conversion substrate and an electric target with wiring.

[0044] Moreover, after grinding and embedding a magnification conversion substrate from a rear-face side and exposing wiring, a magnification conversion substrate is also connectable [a magnification conversion substrate is formed in the image-sensors section by polish and lamination like the gestalt of the above-mentioned implementation, and] with a data storage substrate and an electric target with wiring. Moreover, after grinding and embedding a data storage substrate from a rear-face side and exposing wiring, a data storage substrate is also connectable [a magnification conversion substrate and a data storage substrate are formed in the image-sensors section by polish and lamination like the gestalt of the above-mentioned implementation, and] with a data-processing substrate and an electric target with wiring. Moreover, after grinding and embedding a data-processing substrate from a rear-face side and exposing wiring, a data-processing substrate is also connectable [a magnification conversion substrate, a data storage substrate, and a data-processing substrate are formed in the image-sensors section by

polish and lamination like the gestalt of the above-mentioned implementation, and] with an output circuit substrate and an electric target with wiring.
[0045] In addition, a wafer scale or a chip scale is sufficient as the silicon substrate used in the gestalt of the above-mentioned implementation.
[0046]
[Effect of the Invention] The manufacture approach of the three-dimension image processing system of this invention does so the effectiveness that the attachment-and-detachment process of a support substrate can be unnecessary, can simplify a production process substantially, and can manufacture a three-dimension image processing system according to a simple and easy process. Moreover, the manufacture approach of the three-dimension image processing system of this invention does so the effectiveness surrounded by the reliable insulator layer that it can embed and wiring can be formed.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the outline sectional view showing the production process of the three-dimension image formation equipment of the gestalt of this operation.
[Drawing 2] It is the outline sectional view showing the production process of the three-dimension image formation equipment of the gestalt of this operation.
[Drawing 3] It is the outline sectional view showing the production process of the three-dimension image formation equipment of the gestalt of this operation.
[Drawing 4] It is the outline sectional view showing the production process of the three-dimension image formation equipment of the gestalt of this operation.
[Drawing 5] It is the outline sectional view showing the production process of the three-dimension image formation equipment of the gestalt of this operation.
[Drawing 6] It is the outline sectional view showing the structure of the three-dimension image formation equipment of the gestalt of this operation.
[Description of Notations]
10 Transparence Substrate
12 Micro Lens
16 N Mold Silicon Crystal Substrate
18 P Mold Impurity Layer
20 Photo-Electric-Translation Substrate
22 N Mold Impurity Layer
26 Gate Electrode
28 Electrode
34 Embedding Wiring
40 Magnification Conversion Substrate
70 Data Storage Substrate
80 Data-Processing Substrate
90 Output Circuit Substrate
100 Output Terminal Section